DIGITAL CIRCUITS & SYSTEMS LAB MANUAL

MADHAV INSTITUTE OF TECHNOLOGY & SCIENCE, GWALIOR

(A Govt. Aided UGC Autonomous Institute Affiliated to RGPV, Bhopal)

Department of Electronics Engineering

LAB MANUAL
SEMESTER-IIIrd
DIGITAL CIRCUITS LABORATORY
Subject Code: 140303/200303

DIGITAL CIRCUITS & SYSTEMS LAB MANUAL

PREFACE

Lab Description: Digital Circuits laboratory

Course Objective: To understand the concept of digital systems, design & analyze the combinational and sequential logic circuits.

Course Outcomes:

After completing the lab, students will be able to:

CO1. Verify the operation of basic logic gates and DE Morgan's theorem using standard combinational logic.

CO2. Construct the basic gates by using universal gates.

CO3. Develop adder &subtractor circuits using their truth table.

CO4. Develop the D, RS and JK flip-flops and verify their operation.

CO5. Design Counters and Registers.

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EXPERIMENT 1

Aim: To Implement logic gates – NAND,AND,NOR,EX-OR,EX-NOR.

Apparatus: Digital trainer kit, Logic gates IC, Connecting wires.

Theory: Logic gates are electronic circuits which perform logical functions on one or more inputs to produce one output. There are seven logic gates. When all the input combinations of a logic gate are written in a series and their corresponding outputs written along them, then this input/output combination is called Truth Table. Various gates and their working are explained here.

AND gate

The AND gate produces a HIGH output when all of the inputs are HIGH. The abbreviation for this gate is AND & the operation is denoted by a dot (**.**). When any of the inputs are LOW, the output is LOW. The standard symbol for an AND gate is shown in figure below along with the associated Truth Table.

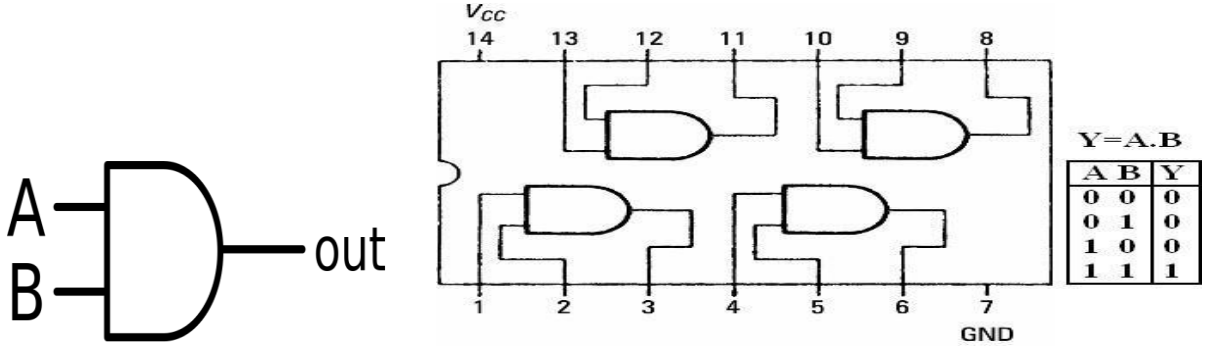


Figure1: IC 7408

OR gate

The OR gate produces a HIGH output when any or all of the inputs is HIGH. The abbreviation for this gate is OR. When both inputs are LOW, the output is LOW. The standard symbol for an OR gate is shown in figure below along with the associated Truth Table. The operation function sign for the OR gate is **(+)**

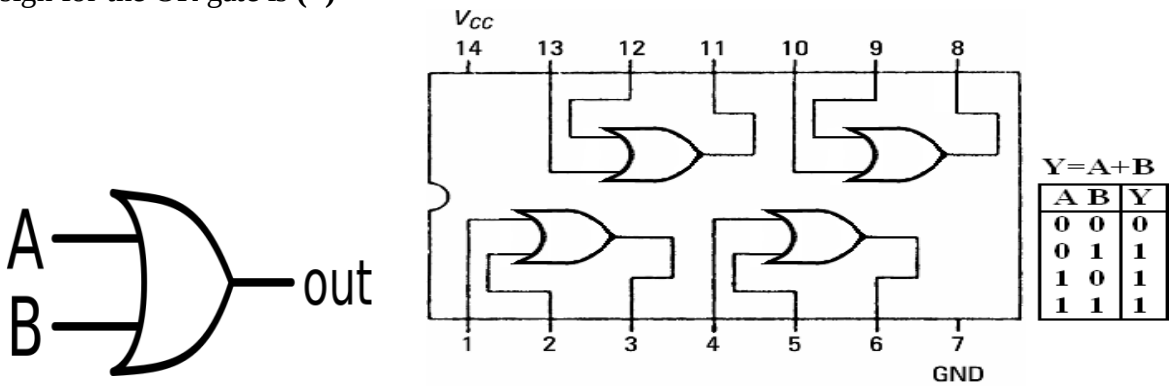


Figure2: IC 7432

NOT gate

NOT gate produces the complement of its input. This gate is also called an INVERTER. It always has one input and one output. Its output is LOW when input is HIGH and output is HIGH

when input is LOW. The standard symbol for an NOT gate is shown in figure below along with the associated Truth Table. The operation function sign for the NOT gate is **(¯ , ')**

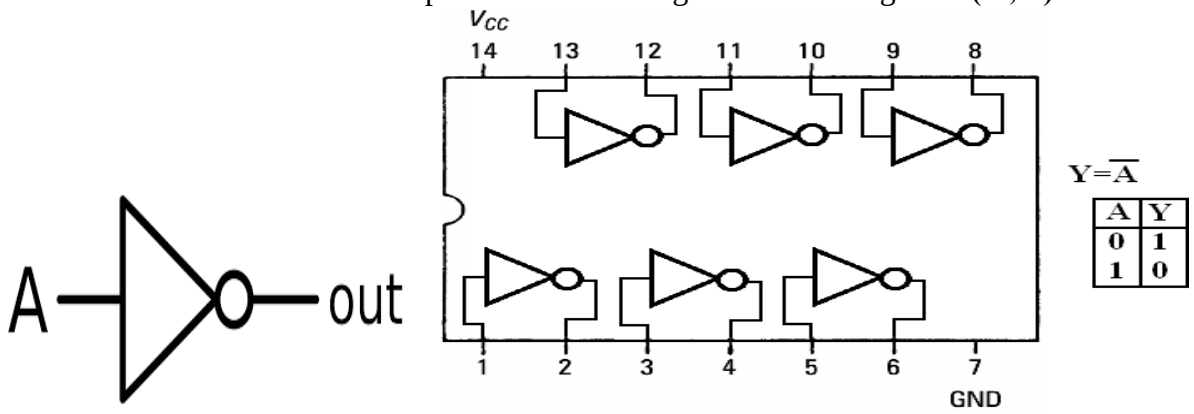


Figure3: IC 7404

NAND gate

The NAND gate produces a LOW output when all of the inputs are HIGH. The abbreviation for this gate is NAND & the operation is same as AND followed with NOT. When any of the inputs are LOW, the output is HIGH. The standard symbol for an NAND gate is shown in figure below along with the associated Truth Table.

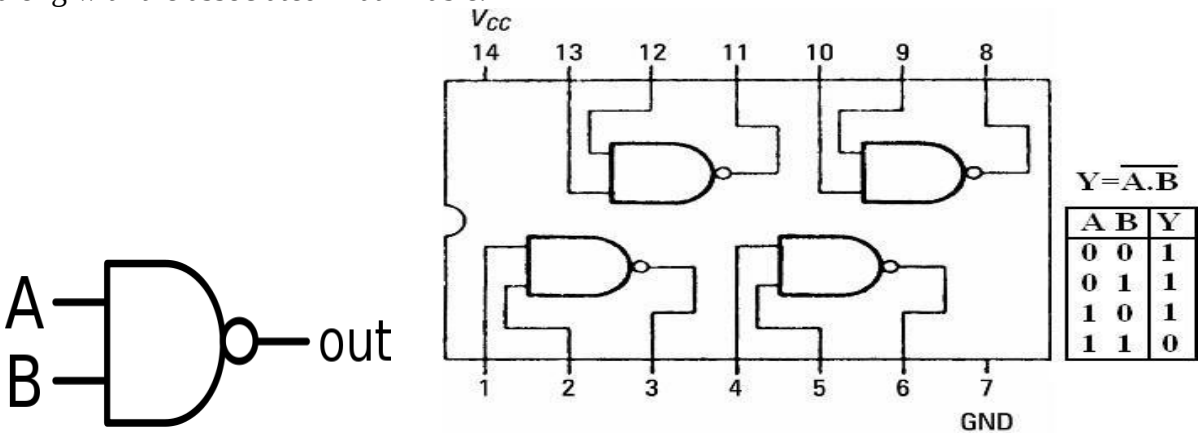
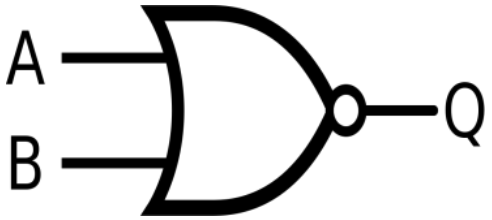


Figure4: IC 7400

NOR gate

The NOR gate produces a HIGH output when all of the inputs are LOW. The abbreviation for this gate is NOR & the operation is same as OR followed with NOT. When any of the inputs are HIGH, the output is LOW. The standard symbol for an NOR gate is shown in figure below along with the associated Truth Table.



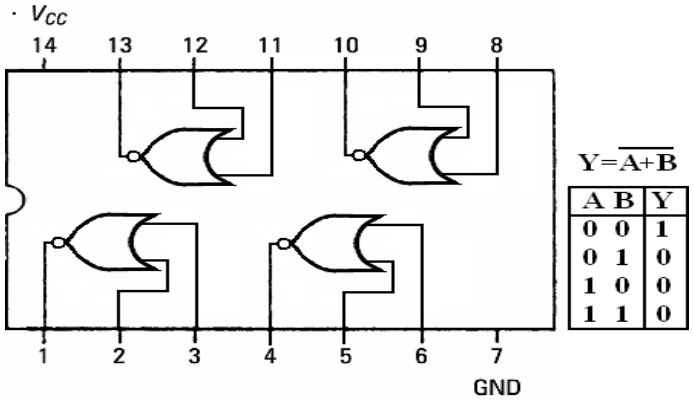
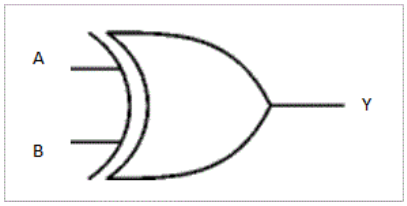


Figure5: IC 7402

Exclusive OR (X-OR) Gate

The exclusive OR gate is a modified OR gate that produces a HIGH output, when number of 1's at its inputs is **odd**, otherwise output is LOW. The standard symbol for an exclusive OR gate is shown in figure below along with the associated Truth Table.



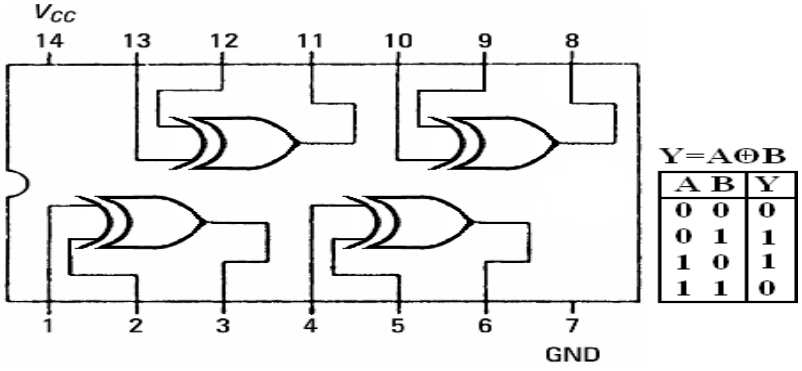
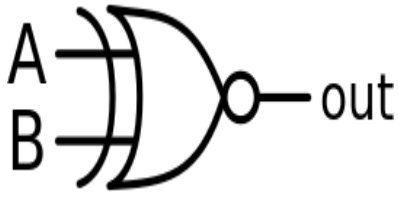


Figure6: IC 7486

Exclusive NOR (X-NOR) Gate

The exclusive NOR gate is a modified OR gate that produces a HIGH output, when number of 1's at its inputs are **even**, otherwise output is LOW. The standard symbol for an exclusive NOR gate is shown in figure below along with the associated Truth Table.



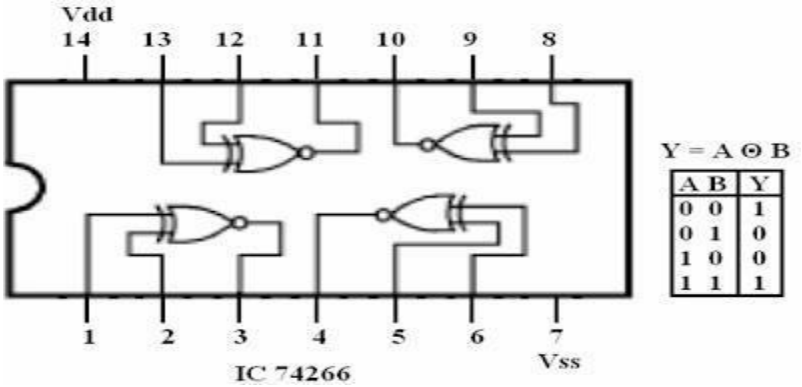


Figure7: IC 74266

Procedure:

1. Place the breadboard gently on the observationtable.
2. Fix the IC which is under observation between the half shadow lineof breadboard, so there is no shortage ofvoltage.
3. Connect the wire to the main voltage source (V_{cc}) whose other end is connected to last pin of the IC (14 place from thenotch).
4. Connect the ground of IC (7_{th} place from the notch) to the ground terminal provided on the digital labkit.
5. Give the input at any one of the gate of the ICs i.e. 1_{st}, 2_{nd}, 3_{rd}, 4_{th} gate by using connecting wires.(In accordance to ICprovided).
6. Connect output pins to the led on digital lab kit.
7. Switch on the powersupply.
8. If led glows then output is true, if it doesn't glow output is false, which is numerically denoted as 1 and 0respectively.
9. Verify the truthtable.

Precautions:

1. All ICs should be checked before starting theexperiment.
2. All the connection should betight.
3. Always connect ground first and then connectVcc.
4. Suitable type wire should be used for different types ofcircuit.
5. The kit should be off before changing theconnections.
6. after the completion of experiment, switch off the supply of theapparatus.

Result: Thus the truth tables for logic gates are verified.

Questions:-

1. What is a logicgate?
   Ans: Logic gate is a physical device implementing a Boolean function and performs Logical operation on one or more logic inputs and produces a single logic output.

2. What are universal gates?
   Ans: NAND and NOR gates are called universal gates as any type of logic gates or logic Functions can be implemented by these gates.

3. What are basicgates?
   Ans: AND, OR, Not are called basic gates.

4. When the output of a NOR gate is high?
   Ans : If all the inputs arelow

EXPERIMENT 2

Aim: To realize basic logic gates using universal gates

Apparatus: Digital trainer kit, IC 7400, IC 7402, Connecting wires.

Theory: A universal gate is a gate which can implement any Boolean function without need to use any other gate type. The NAND and NOR gates are universal gates. In practice, this is advantageous since NAND and NOR gates are economical and easier to fabricate.

NAND gate

The NAND gate produces a LOW output when all of the inputs are HIGH. The abbreviation for this gate is NAND & the operation is same as AND followed with NOT. When any of theinputs are LOW, the output is HIGH. The standard symbol for an NAND gate is shown in figure below along with the associated TruthTable.

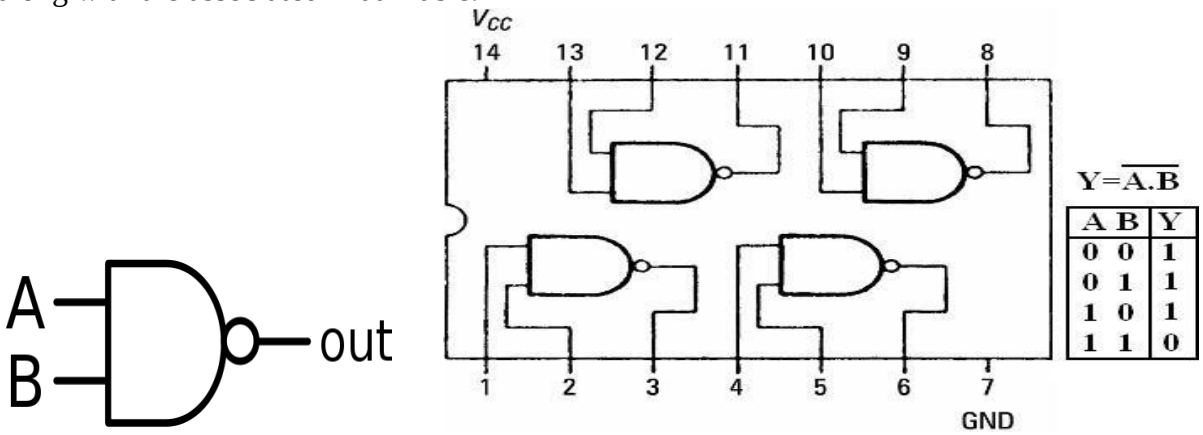


Figure1: IC 7400

NOR gate

The NOR gate produces a HIGH output when all of the inputs are LOW. The abbreviation for this gate is NOR & the operation is same as OR followed with NOT. When any of the inputs are HIGH, the output is LOW. The standard symbol for an NOR gate is shown in figure below along with the associated Truth Table.

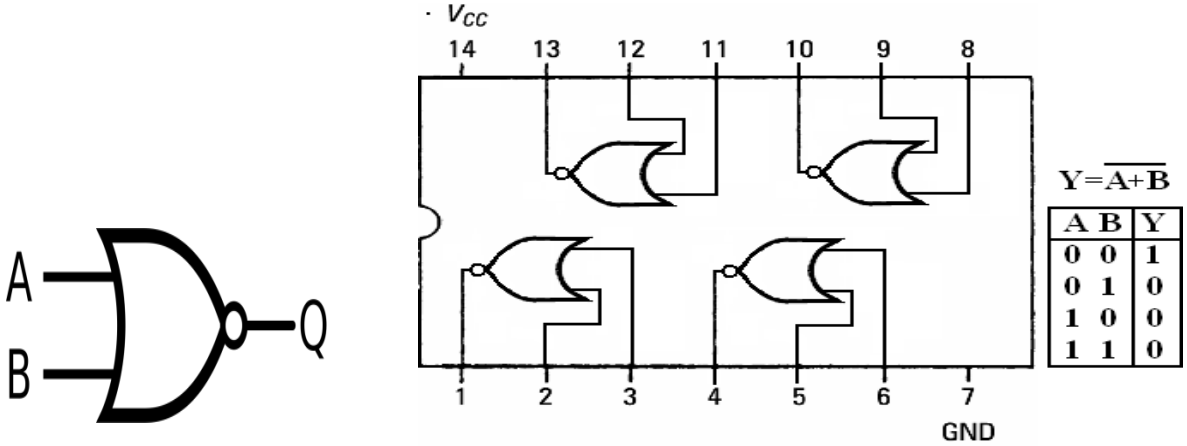


Figure2: IC 7402

NAND Gate as a Universal Gate

To prove that any Boolean function can be implemented using only NAND gates, we will show that the AND, OR, and NOT operations can be performed using only these gates.

Implementing an Inverter Using only NAND Gate

A NOT produces complement of the input. It can have only one input, tie the inputs of a NAND gate together. Now it will work as a NOT gate. Its output is

$$Y = (A.A)'$$

$$\Rightarrow \quad Y = (A)'$$

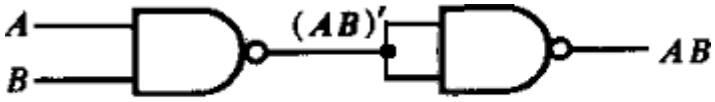
NOT (inverter)

Implementing AND Using only NAND Gates

A NAND produces complement of AND gate. So, if the output of a NAND gate is inverted, overall output will be that of an AND gate.

$$Y = ((A.B)')'$$

$$\Rightarrow \quad Y = (A.B)$$



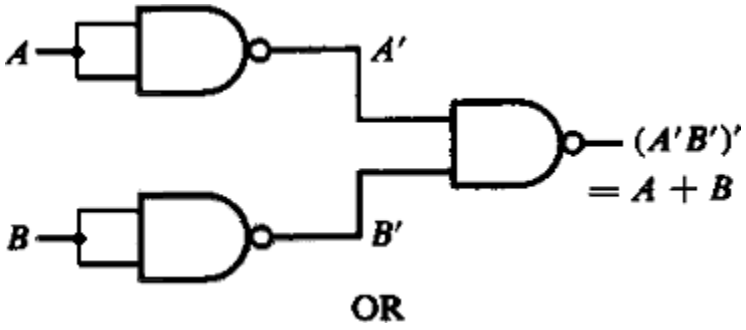
AND

Implementing OR Using only NAND Gates

From DeMorgan's theorems: $(A.B)' = A' + B'$

$$\Rightarrow \quad (A'.B')' = A'' + B'' = A + B$$

So, give the inverted inputs to a NAND gate, obtain OR operation at output



OR

NOR Gate as a Universal Gate

To prove that any Boolean function can be implemented using only NOR gates, we will show that the AND, OR, and NOT operations can be performed using only these gates.

Implementing an Inverter Using only NOR Gate

A NOT produces complement of the input. It can have only one input, tie the inputs of a NOR gate together. Now it will work as a NOT gate. Its output is

Y = (A+A)'

=> Y =(A)'

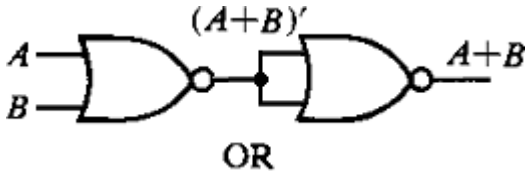
NOT

Implementing OR Using only NOR Gates

A NOR produces complement of OR gate. So, if the output of a NOR gate is inverted, overall output will be that of an OR gate.

Y = ((A+B)')'

=> Y =(A+B)



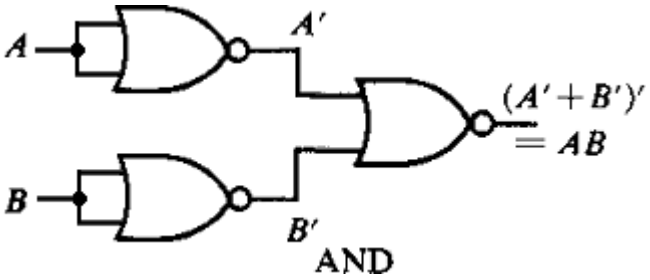
OR

Implementing AND Using only NOR Gates

From DeMorgan's theorems: (A+B)' = A'B'

=> (A'+B')' = A''B'' =AB

So, give the inverted inputs to a NOR gate, obtain AND operation at output.



AND

Procedure:

1. Place the breadboard gently on the observationtable.
2. Fix the IC which is under observation between the half shadow lineof breadboard, so there is no shortage ofvoltage.
3. Connect the wire to the main voltage source (V_{cc}) whose other end is connected to last pin of the IC (14 place from thenotch).
4. Connect the ground of IC (7_{th} place from the notch) to the ground terminal provided on the digital labkit.
5. Give the input at any one of the gate of the ICs by using connecting wires. (Inaccordance to ICprovided).
6. Connect output pins to the led on digital labkit.
7. Switch on the powersupply.
8. If led glows then output is true, if it doesn't glow output is false, which is numerically denoted as 1 and 0respectively.
9. Verify the truthtable.

Precautions:

1. All ICs should be checked before starting theexperiment.
2. All the connection should betight.
3. Always connect ground first and then connectVcc.
4. Suitable type wire should be used for different types ofcircuit.
5. The kit should be off before changing theconnections.
6. after the completion of experiment, switch off the supply of theapparatus.

Result: Thus the basic logic gates using universal gates are realized and the truth table is verified.

Questions:-

1. What are universal gates?
   Ans: NAND and NOR gates are called universal gates as any type of logic gates or logic Functions can be implemented by these gates.

2. When the output of a NOR gate is high?
   Ans : If all the inputs arelow

3. State De-Morgan'stheorem.
   Ans: $(x+y)' = x'y'$
   $(xy)' = x' + y'$

EXPERIMENT 3

Aim: To verify the truth table of half adder and full adder

Apparatus: Digital trainer kit, IC 7486, IC 7432, IC 7408, Connecting wires.

Theory: Adder circuit is a combinational digital circuit that is used for adding two numbers. A typical adder circuit produces a sum bit (denoted by S) and a carry bit (denoted by C) as the output. Adder circuits can be used for a lot of other applications in digital electronics like address decoding, table index calculation etc. Adder circuits are of two types: Half adder ad Full adder

HALF ADDER

A half adder is a combinational circuit that performs the sum of two binary digits (A, B) to givea maximum of two binary outputs namely the sum(S) and the carry(C). Carry is the higher order bitand the sum is the lower order bit of the output. Functional Table of the Half-Adder is given below

A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Table: Functional Table of Half Adder

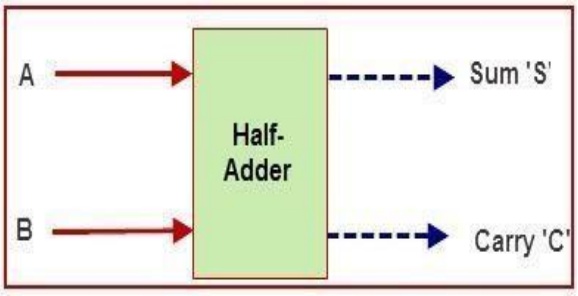


Figure1: Half adder block diagram

The Boolean expression for the sum (S) and carry(C) of half adder is,

SUM = AB' + A'B = A⊕B

CARRY= A.B

FULL ADDER

A full adder is a combinational circuit that performs the sum of three binary digits (A, B, Cin) to give a maximum of two binary outputs namely the sum(S) and the carry- out (Cout).The full adder becomes necessary when a carry input must be added to the two binary digits to obtain the correct sum. A half adder has no input for carries from previous circuits

A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table: Functional Table Full Adder

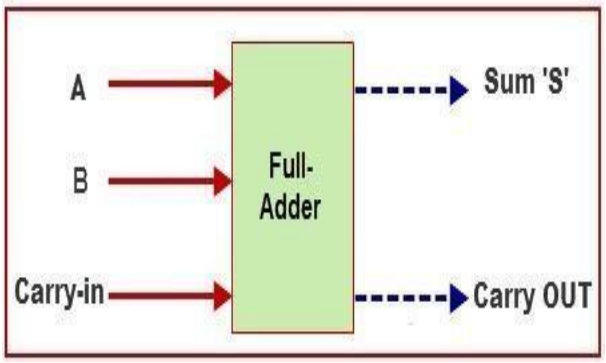


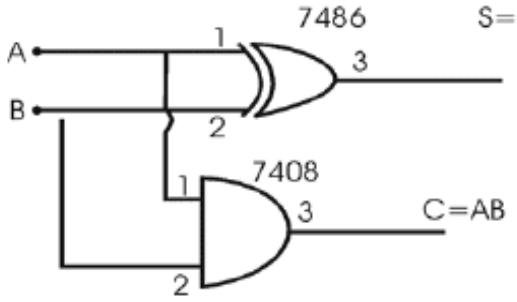
Figure2: full adder block diagram

The Boolean expression for the sum (S) and carry-out (Cout) of full adder is,
SUM = A'B'C + A'BC' + AB'C' + ABC
Cout = A'BC + AB'C + ABC' + ABC

SIMPLIFICATION OF LOGIC EQUATIONS

SUM = A'B'C + A'BC' + AB'C' + ABC
= A'(B'C+BC') + A(B'C'+BC)
=A ⊕B ⊕C
Cout = A'BC + AB'C + ABC' +ABC
= A'BC + ABC+ AB'C +ABC'
= AB(C+C') + C(A'B+AB')
= AB + C(A ⊕B)

Half Adder using basic gates:-



$S = \overline{A}B + A\overline{B}$

$S = A \oplus B$

$C = AB$

Full Adder using basic gates:-

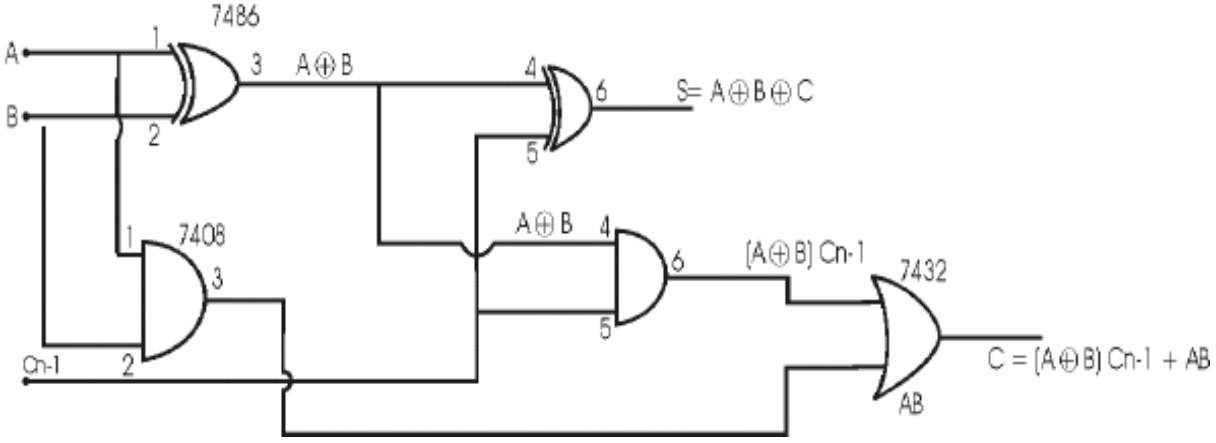


Figure3: Half & full adder logic diagram

The full adder drawn above can be visualized as a combination of two half adders. It uses two XOR gates, the output of 1st XOR gate (i.e. SUM A+B) is taken as input to 2nd XOR gate and the other is the third input(usually the Cin), the outputs of the AND gates which are nothing but the carry of HA are ORed together. The FA drawn as a combination of two HA is shown below.

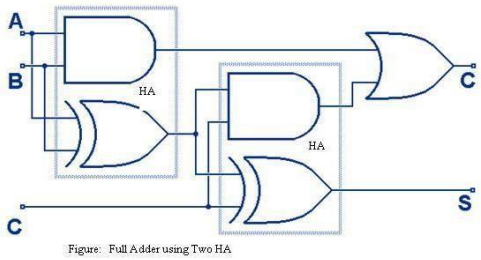


Figure: Full Adder using Two HA

Procedure:

1. Place the breadboard gently on the observationtable.
2. Fix the IC which is under observation between the half shadow lineof breadboard, so there is no shortage ofvoltage.
3. Connect the wire to the main voltage source (V_{cc}) whose other end is connected to last pin of the IC (14 place from thenotch).
4. Connect the ground of IC (7_{th} place from the notch) to the ground terminal provided on the digital labkit.
5. Give the input at the gate of the ICs by using connecting wires. (In accordance to IC provided).
6. Connect output pins to the led on digital lab kit.
7. Switch on the powersupply.
8. If led glows then output is true, if it doesn't glow output is false, which is numerically denoted as 1 and 0respectively.
9. Verify the truthtable.

Precautions:

1. All ICs should be checked before starting theexperiment.
2. All the connection should betight.
3. Always connect ground first and then connectVcc.
4. Suitable type wire should be used for different types ofcircuit.
5. The kit should be off before changing theconnections.
6. after the completion of experiment, switch off the supply of theapparatus.

Result: The truth table of half adder and full adder is verified.

Questions:-

1. What is a combinationalcircuit?
   Ans: In a combinational circuit, the output depends upon present input(s) only i.e, not dependant on the previous input(s). The combinational circuit has no memory element. It consists of logic gates only

2. What is ahalf-adder?
   Ans: A logic circuit, that can add two 1-bit numbers and produce outputs for sum and carry, is called a half-adder.

3. What is afull-adder?
   Ans: A binary adder, which can add two 1-bit binary numbers along with a carry bit and produces outputs for sum and carry is called a full-adder.

EXPERIMENT 4

Aim: To verify the truth table of half and full subtractor

Apparatus: Digital trainer kit, IC 7486, IC 7432, IC 7408, IC 7404 Connecting wires.

Theory: Binary Subtractor is a decision making circuit that subtracts two binary numbers from each other, for example, X – Y, the resulting output binary subtractor produces is a DIFFERENCE, D by using a BORROW bit, B from the previous column.

HALF SUBTRACTOR

A half subtractor is a logical circuit that performs a subtraction operation on two single binary digits. The half subtractor produces a difference and a borrow bit for the next stage.

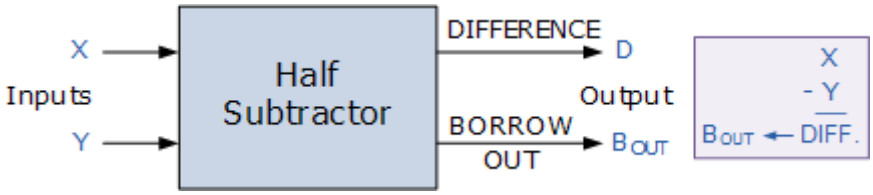
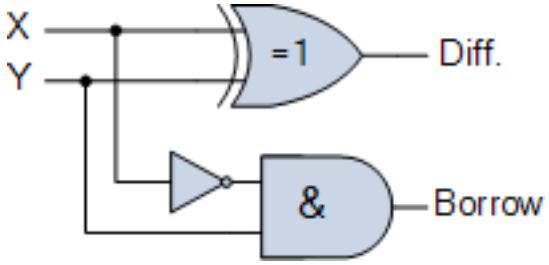


Figure1: Half subtractor block diagram



Inputs		Outputs	
X	Y	D	B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Figure2: Half subtractor logic diagram

From the truth table of the half subtractor we can see that the DIFFERENCE (D) output is the result of the Exclusive-OR gate and the Borrow-out (B) is the result of the NOT-AND combination. Then the Boolean expression for a half subtractor is as follows.

For the **DIFFERENCE** bit:
D = X XOR Y = X $\oplus$ Y

For the **BORROW** bit
B = not-X AND Y = X.Y

FULL SUBTRACTOR

A full subtractor has three inputs. The two single bit data inputs X (minuend) and Y(subtrahend) the same as before plus an additional *Borrow-in* (B-in) input to receive the borrow generated by the subtraction process from a previous stage as shown below.

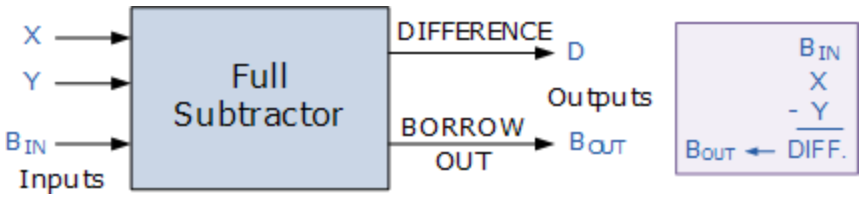
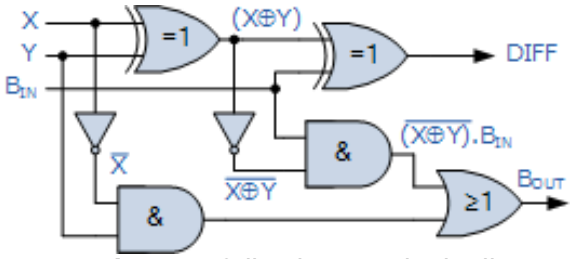


Figure3: full subtractor block diagram



Inputs			Outputs	
X	Y	Z	D	B
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Figure4: full subtractor logic diagram

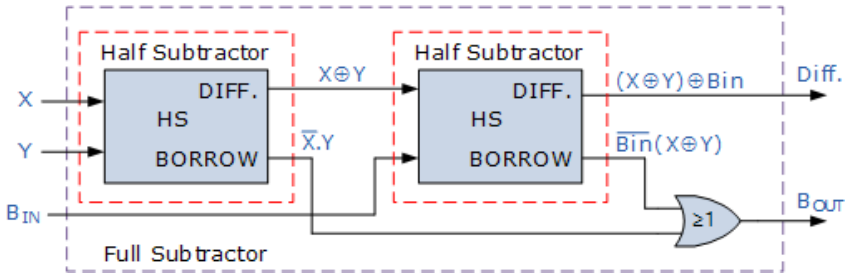


Figure5: full subtractor using Halfsubtractor diagram

For the **DIFFERENCE** (D) bit:
$D = (X'.Y'.B_{IN}) + (X'.Y.B_{IN}') + (X.Y'.B_{IN}') + (X.Y.B_{IN})$
which can be simplified too:
$D = (X \text{ XOR } Y) \text{ XOR } B_{IN} = (X \oplus Y) \oplus B_{IN}$

For the **BORROW OUT** (B_{OUT}) bit:
$B_{OUT} = (X'.Y'.B_{IN}) + (X'.Y.B_{IN}') + (X'.Y.B_{IN}) + (X.Y.B_{IN})$
which will also simplify too:
$B_{OUT} = X' \text{ AND } Y \text{ OR } (X \text{ XOR } Y)'B_{IN} = X'.Y + (X \oplus Y)'B_{IN}$

Procedure:

1. Place the breadboard gently on the observationtable.
2. Fix the IC which is under observation between the half shadow lineof breadboard, so there is no shortage ofvoltage.
3. Connect the wire to the main voltage source (V_{cc}) whose other end is connected to last pin of the IC (14 place from thenotch).
4. Connect the ground of IC (7_{th} place from the notch) to the ground terminal provided on the digital labkit.
5. Give the input at the gate of the ICs by using connecting wires. (In accordance toIC provided).
6. Connect output pins to the led on digital labkit.
7. Switch on the powersupply.

8. If led glows then output is true, if it doesn't glow output is false, which is numerically denoted as 1 and 0respectively.
9. Verify the truthtable.

Precautions:

1. All ICs should be checked before starting theexperiment.
2. All the connection should betight.
3. Always connect ground first and then connectVcc.
4. Suitable type wire should be used for different types ofcircuit.
5. The kit should be off before changing theconnections.
6. after the completion of experiment, switch off the supply of theapparatus.

Result: The truth table of half subtractor and full subtractor is verified.

Questions:-

1. What is a combinationalcircuit?
   Ans: In a combinational circuit, the output depends upon present input(s) only i.e, not dependant on the previous input(s). The combinational circuit has no memory element. It consists of logic gates only

2. What is ahalf-subtractor?
   Ans: A logic circuit, that can subtracts two 1-bit numbers and produce outputs for difference and borrow, is called a half- subtractor.

3. What is a full-subtractor?
   Ans: A binary subtractor, which can subtracts two 1-bit binary numbers along with a borrow bit and produces outputs for difference and borrow is called a full- subtractor.

EXPERIMENT 5

Aim: To design R-S FlipFlop

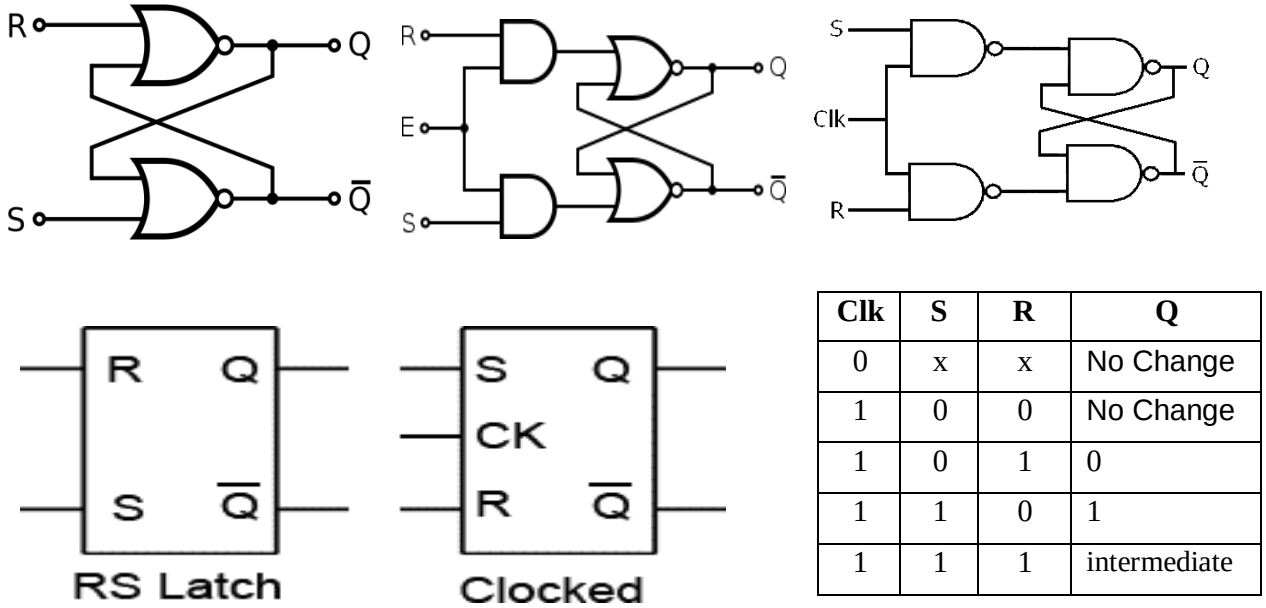
Apparatus: Digital trainer kit, IC 7400, IC 7402, IC 7408, Connecting wires.

Theory: The logic circuits that incorporate memory cells are called *sequential logic circuits*; their output depends not only upon the present value of the input but also upon the previous values. Sequential logic circuits often require a timing generator (a clock) for their operation. Flip flops are actually an application of logic gates. With the help of Boolean logic you can create memory with them. Flip flops can also be considered as the most basic idea of a Random Access Memory [RAM]. When a certain input value is given to them, they will be remembered and executed, if the logic gates are designed correctly. Usually there are two outputs, Q and its complementaryvalue.

R-S Flip-Flop

The fundamental latch is the simple SR latch, where S and R stand for set and reset respectively. It can be constructed from a pair of cross-coupled NOR logic gates. The stored bit is present on the output marked Q. Normally, in storage mode, the S and R inputs are both low, & feedback maintains the outputs in a constant state, with Q and the complement of Q. If S (Set) is given with high while R is held low, then the Q output is forced high; similarly, if R (Reset) is given with high while S is held low, then the Q output is forced low. For S & R both high, output is invalid. It is an invalid state because the values of both Q and Q' are 0. They are supposed to be compliments of each other. Normally, this state must be avoided.

Latch usingNOR gate **S-R Flip-flop using NOR gate** **S-R Flip-flop using NAND gate**



Clk	S	R	Q
0	x	x	No Change
1	0	0	No Change
1	0	1	0
1	1	0	1
1	1	1	intermediate

Figure1: S R flip-flop block diagram & logic circuit

A clock pulse [CLK] is given to the inputs of the AND Gate. When the value of the clock pulse is '0', the outputs of both the AND Gates remain '0'. As soon as a pulse is given the value of CLK turns '1'. This makes the values at S and R to pass through the NOR Gate flip flop.

Procedure:

1. Place the breadboard gently on the observationtable.
2. Fix the IC which is under observation between the half shadow lineof breadboard, so there is no shortage ofvoltage.
3. Connect the wire to the main voltage source (V_{cc}) whose other end is connected to last pin of the IC (14 place from thenotch).
4. Connect the ground of IC (7_{th} place from the notch) to the ground terminal provided on the digital labkit.
5. Give the input at the gate of the ICs by using connectingwires.
6. Connect output pins to the led on digital lab kit.
7. Switch on the powersupply.
8. If led glows then output is true, if it doesn't glow output is false, which is numerically denoted as 1 and 0respectively.
9. The values of the outputs aretabulated.

Precautions:

1. All ICs should be checked before starting theexperiment.
2. All the connection should betight.
3. Always connect ground first and then connectVcc.
4. Suitable type wire should be used for different types ofcircuit.
5. The kit should be off before changing theconnections.
6. after the completion of experiment, switch off the supply of theapparatus.

Result: S-R flip-flop is designed and its truth table is verified.

Questions:-

1) What is alatch?
Ans: Storage elements that operate with signal levels are referred to as latches.

2) What is a flipflop?
Ans: Storage elements controlled by a clock transitions are called flip flop.

3) Differentiate between a latch and a flipflop.
Ans: A latch checks all its inputs continuously and changes its outputs accordingly at anytime. Flip flop samples its inputs and changes its outputs only at a time as determined by a clocking signal.

4) Differentiate between combinational and sequentialcircuits.
Ans: Combinational Circuits: *A circuit whose output is * Easy to design * Does not use memory element
Sequential Circuits: *Dependent only on the inputs at that instant * It depends on present and past history of the inputs * requires the Memory Elements

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EXPERIMENT 6

Aim: To design J-KFlip-Flop

Apparatus: Digital trainer kit, IC 7411, IC 7402, Connecting wires.

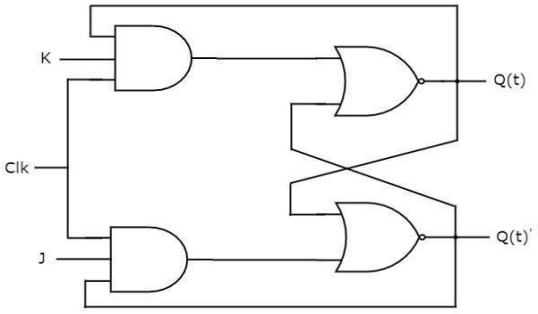
Theory: The logic circuits that incorporate memory cells are called *sequential logic circuits*; their output depends not only upon the present value of the input but also upon the previous values. Sequential logic circuits often require a timing generator (a clock) for their operation. Flip flops are actually an application of logic gates. With the help of Boolean logic you can create memory with them. Flip flops can also be considered as the most basic idea of a Random Access Memory [RAM]. When a certain input value is given to them, they will be remembered and executed, if the logic gates are designed correctly. Usually there are two outputs, Q and its complementaryvalue.

J-K Flip-Flop

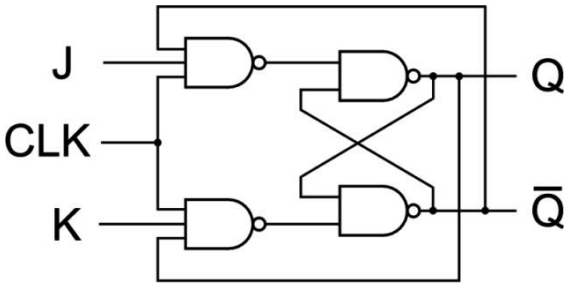
A J-K flip flop can also be defined as a modification of the S-R flip flop. The only difference is that the intermediate state is more refined and precise than that of a S-R flip flop. The behavior of inputs J and K is same as the S and R inputs of the S-R flip flop. When both the inputs J and K have a HIGH state, the flip-flop switches to the complement state. So, for a value of Q = 1, it switches to Q=0 and for a value of Q = 0, it switches toQ=1.

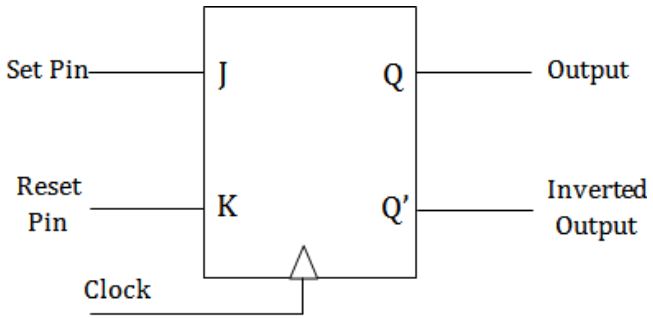
The output may be repeated in transitions once they have been complimented for J=K=1 because of the feedback connection in the JK flip-flop. This can be avoided by setting a time duration lesser than the propagation delay through the flip-flop. The restriction on the pulse width can be eliminated with a master-slave or edge-triggered construction.

J-K Flip-flop usingNORgates



J-K Flip-flop using NANDgates





Symbol: JK Flip-flop

Clk	J	K	Q
0	x	x	No Change
1	0	0	No Change
1	0	1	0
1	1	0	1
1	1	1	Toggle

Figure1: J K flip-flop block diagram & logic circuit

The combination J = 1, K = 0 is a command to set the flip-flop; the combination J = 0, K = 1 is a command to reset the flip-flop; and the combination J = K = 1 is a command to toggle the flip-flop, i.e., change its output to the logical complement of its current value.

Procedure:

1. Place the breadboard gently on the observationtable.
2. Fix the IC which is under observation between the half shadow lineof breadboard, so there is no shortage ofvoltage.
3. Connect the wire to the main voltage source (V_{cc}) whose other end is connected to last pin of the IC (14 place from thenotch).
4. Connect the ground of IC (7_{th} place from the notch) to the ground terminal provided on the digital labkit.
5. Give the input at the gate of the ICs by using connectingwires.
6. Connect output pins to the led on digital lab kit.
7. Switch on the powersupply.
8. If led glows then output is true, if it doesn't glow output is false, which is numerically denoted as 1 and 0respectively.
9. The values of the outputs aretabulated.

Precautions:

1. All ICs should be checked before starting theexperiment.
2. All the connection should betight.
3. Always connect ground first and then connectVcc.
4. Suitable type wire should be used for different types ofcircuit.
5. The kit should be off before changing theconnections.
6. after the completion of experiment, switch off the supply of theapparatus.

Result: J-K flip-flop is designed and its truth table is verified.

Questions:-

1. How is a J-K flip-flop made totoggle?
   Ans: When j=k=1 then the race condition is occurs that means both output wants to be HIGH. Hence, there toggle condition is occurs.

2. A J-K flip-flop with J = 1 and K = 1 has a 20 kHz clock input. The Q output is?
   Ans: The flip flop is sensitive only to the positive or negative edge of the clock pulse. So, the flip-flop toggles whenever the clock is falling/rising at edge. Thus, the output curve has a time period twice that of the clock. Frequency is inversely related to time period and hence frequency gets halved, so a 10 kHz square wave

3. What is the significance of the J and K terminals on the J-Kflip-flop?
   Ans: The letters J & K were chosen in honour of Jack Kilby, the inventory of the integrated circuit.

EXPERIMENT 7

Aim: To examine parity generator/checker circuit.

Apparatus: Digital trainer kit, IC 7486, IC 7400, Connecting wires.

Theory: A parity bit is used for the purpose of detecting errors during transmission of binary information. A parity bit is an extra bit included with a binary message to make the number of 1's either odd or even. The message including the parity bit istransmitted and then checked at the receiving end for errors. An error is detected if the checked parity does not correspond with the one transmitted. The circuit that generates the parity bit in the transmitter is called a parity generator and the circuit that checks the parity in the receiver is called a parity checker. In odd parity the added parity bit will make the total number of 1's an oddamount.

In a three bit odd parity generator the three bits in the message together with the parity bit are transmitted to their destination, where they are applied to the parity checker circuit. The parity checker circuit checks for possible errors in the transmission

Since the information was transmitted with odd parity the four bits received must have an odd number of 1's. An error occurs during the transmission if the four bits received have an even number of 1's, indicating that one bit has changed during transmission. The output of the parity checker is denoted by PEC (parity error check) and it will be equal to 1 if an error occurs, i.e., if the four bits received has an even number of 1's

ODD PARITY GENERATOR

INPUT (Three bit message)			OUTPUT (Odd Parity bit)
A	**B**	**C**	**P**
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

From the truth table the expression for the output parity bit is,

P (A, B, C) = Σ m (0, 3, 5, 6) Also written as,

$$P = \bar{A}\bar{B}\bar{C} + \bar{A}BC + A\bar{B}C + AB\bar{C}$$

$$P = \overline{(A \oplus B \oplus C)}$$

CIRCUIT DIAGRAM: ODD PARITY GENERATOR

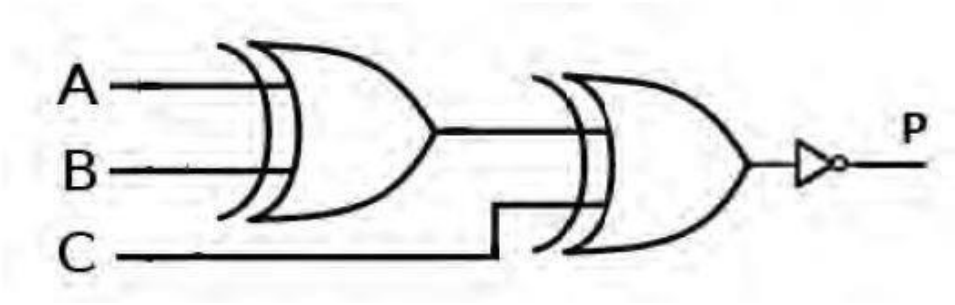


Figure1: Odd parity generator

ODD PARITY CHECKER

INPUT (four bit messageReceived)				**OUTPUT** (Parity error check)
A	**B**	**C**	**P**	**X**
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

From the truth table the expression for the output parity checker bit is,
X (A, B, C, P) = Σ (0, 3, 5, 6, 9, 10, 12, 15)

The above expression is reduced as,

$$X = \overline{(A \oplus B \oplus C \oplus P)}$$

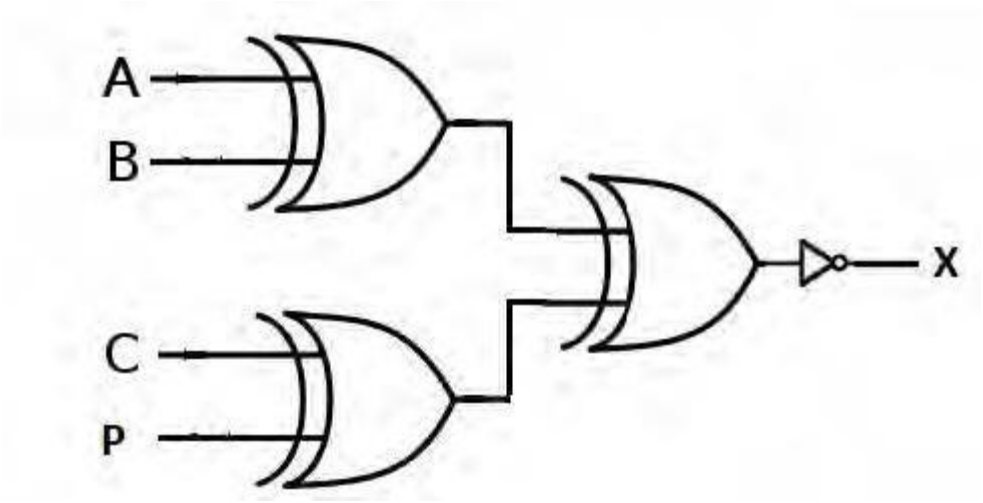


Figure2: Odd parity checker

Procedure:

1. Connections are given as per the circuitdiagrams.
2. for all the ICs 7th pin is grounded and 14th pin is given +5 Vsupply.
3. Apply the inputs and verify the truth table for the Parity generator andchecker.

Precautions:

1. All ICs should be checked before starting theexperiment.
2. All the connection should betight.
3. Always connect ground first and then connectVcc.
4. Suitable type wire should be used for different types ofcircuit.
5. The kit should be off before changing theconnections.
6. after the completion of experiment, switch off the supply of theapparatus.

Result: The design of the three bit odd Parity generator and checker circuits was done and their truth tables were verified.

Questions:-

1) Which error detection method uses one's complementarithmetic?

Ans: A checksum can be generated simply by adding bits. Hence, one's complement arithmeticuses checksum.

2) Which error detection method consists of just one redundant bit per data unit?Ans: Simple parity check method consists of just one redundant bit per dataunit.

3) How many types of parity bits arefound?

Ans: There are two types of parity bits, namely even parity and odd parity.

4) What is a paritybit?

Ans: A simple form of error detection is achieved by adding an extra bit to the transmitted

word.The additional bit is known as parity bits.

EXPERIMENT 8

Aim: To design ripple counter using J-K Flip-Flop

Apparatus: Digital trainer kit, IC 7476, Connecting wires.

Theory: A counter is a sequential circuit that moves through a predefined sequence of states upon applying of clock pulses. The sequence of states may follow the binary number sequence or an arbitrary manner (no sequence). The simplest example of a counter is the binary counter which follows the binary number sequence. An n-bit binary counter contains n flip-flops and can count binary numbers from 0 to $(2^n - 1)$. Counters are classified into two types: synchronous counters and asynchronous/ripple counter. In a synchronous counter, all flip flops are triggered by a common pulse (CLK). In the ripple counter a flip flop output used as a signal for triggering other flipflop.

Ripple Counter (Asynchronous)

A ripple counter is a serial counter. The clock input is applied to only the first of the series of the Flip Flop. Clock pulses for the other Flip Flop come from the preceding Flip Flop. Thus, the clock pulse "ripple" through the circuit in a series fashion. Such circuit is also called asynchronous since the only pulse required for the operation is the clock pulse. The JK Flip Flop have the J and K inputs both tied high, which allows them to toggle with each inputpulse.

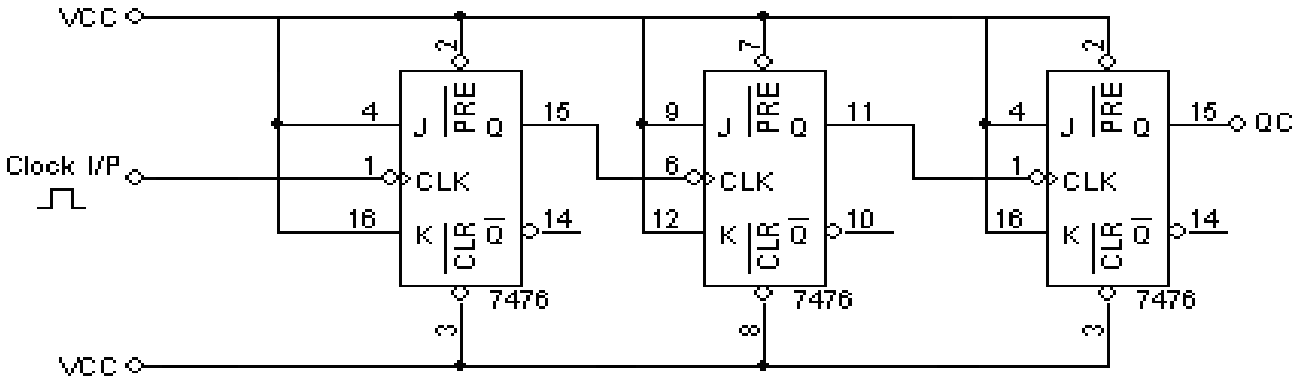


Figure1: 3 bit ripple counter

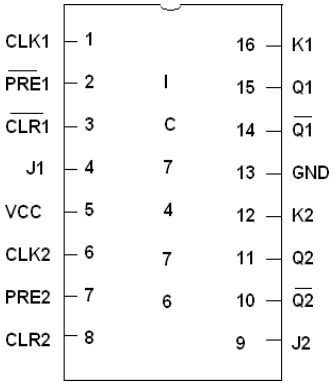


Figure1: Pin diagram of IC 7476

CLK	Q_C	Q_B	Q_A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0

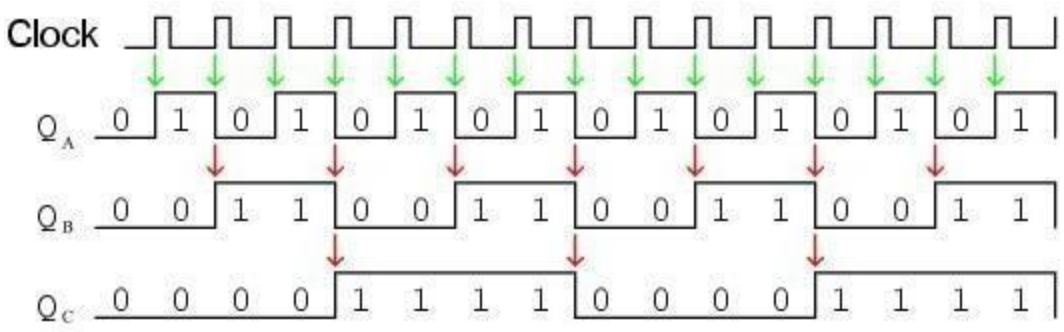


Figure3: Output waveform

Procedure:

1. Place the breadboard gently on the observationtable.
2. Fix the IC which is under observation between the half shadow lineof breadboard, so there is no shortage ofvoltage.
3. Connections are made as per the circuitdiagram
4. Switch on the powersupply.
5. Apply clock pulses at clock input of IC and note the outputs after each clock pulse. O/Pis observed at QA, QB & QC for IC7476.

Precautions:

1. All ICs should be checked before starting theexperiment.
2. All the connection should betight.
3. Always connect ground first and then connectVcc.
4. Suitable type wire should be used for different types ofcircuit.
5. The kit should be off before changing theconnections.
6. afterthe completionofexperiment,switchoffthesupplyoftheapparatus.

Result: Ripple counter using J-K Flip-Flop is designed and its truth table isverified.

Questions:-

1) What is an asynchronouscounter?
Ans: Asynchronous counter is one in which flip flops are connected in such a way that the first flip flop output is the clock for the nest flip flop.

2) What is the major drawback of asynchronouscounters?
Ans: High frequency applications are limited because of internal propagation delay.

3) How many different states 2 bit asynchronous counters have?
Ans:4

4) How the up counter can be made to work as a downcounter?
Ans: By taking the counter outputs Q' instead of Q the up counter can be made to work as a down counter.
