MADHAV INSTITUTE OF TECHNOLOGY & SCIENCE, GWALIOR
(Deemed University)
NAAC Accredited with A++ Grade

DEPARTMENT OF ELECTRONICS ENGINEERING

Report Title:- Online Workshop on Circuit Simulation using Cadence

Date:- 31st Aug 2024 (Saturday),

Schedule:- 04:00PM– 05:00 PM

Resource Persons:-

Dr. Ashima Gupta (Analog Design Engineer), Intel Cooperation, Bangalore

Objective of workshop:

- To impart the practical knowledge about simulation of various logic Circuits.
- The main objective of the online workshop was to brief the students about the implementation from basic to advance applications of electronic circuits especially in the field of analog VLSI design.

Objectives

The online workshop on circuit simulation using Cadence was successfully conducted, providing participants with an in-depth understanding of the essential features and functionalities of the Cadence toolset. The session covered the following key areas:

1. **Introduction to Cadence**: Participants were introduced to the Cadence environment, including its interface, toolbars, and primary functions used in circuit design and simulation.
2. **Circuit Design Fundamentals**: The workshop covered the basic principles of circuit design, including schematic entry, component selection, and the creation of circuit layouts.
3. **Simulation Techniques**: Detailed instructions were provided on setting up simulations, selecting appropriate simulation models, and interpreting simulation results. Participants learned how to analyze circuit behavior under different conditions.
4. **Hands-On Practice**: Attendees engaged in practical exercises, where they applied the concepts learned to design and simulate simple circuits using Cadence. This hands-on approach helped reinforce their understanding of the tool.
5. **Q&A Session**: The workshop concluded with an interactive Q&A session, where participants asked questions about the tool and clarified their doubts.

Outcome: Participants gained practical skills in using Cadence for circuit simulation, which they can apply to their own projects. The workshop received positive feedback for its comprehensive coverage and interactive format, indicating a successful learning experience.

Workshop Overview

On 31/08/2024, the workshop was conducted with Dr. Ashima Gupta working as a (Analog Design Engineer) at Intel Cooperation as the resource person. A total of 55 students presents online from the Electronics and Communication (EC) and Electronics and Telecommunication (ET) branches attended the session.

Introduction to Cadence Tool and Simulation of Circuits

Cadence is a leading electronic design automation (EDA) tool widely used in the semiconductor industry for designing and simulating integrated circuits (ICs). It offers a comprehensive suite of tools for schematic capture, layout design, and circuit simulation, enabling engineers to efficiently create and validate complex digital and analog circuits.

Circuit simulation using Cadence allows designers to model and analyze the behavior of logic gates, which are the fundamental building blocks of digital circuits. Through simulation, engineers can verify the functionality of logic gates—such as AND, OR, NOT, NAND, and NOR gates—under various conditions before proceeding to physical implementation, ensuring the design meets the required specifications and operates correctly in real-world applications.

When designing a circuit in Cadence, the following basic steps are typically followed:

1. **Project Setup**: Start by creating a new project or workspace within Cadence. Set up the required libraries and design files that will be used throughout the design process.
2. **Schematic Capture**: Open the schematic editor and begin drawing the circuit by placing components such as resistors, capacitors, transistors, and logic gates from the library onto the schematic. Connect these components using wires to form the desired circuit.
3. **Component Selection and Parameter Setting**: Select the appropriate components from the Cadence library, and configure their properties, such as resistance, capacitance, and transistor sizing, according to the design requirements.
4. **Design Rule Check (DRC)**: Perform a design rule check to ensure that the schematic adheres to the predefined design rules and constraints. This step helps identify any errors or violations in the schematic.
5. **Simulation Setup**: Set up the simulation environment by choosing the type of simulation (e.g., DC, AC, transient), defining the input sources, and specifying the analysis parameters. Assign appropriate simulation models to the components.
6. **Running Simulations**: Run the simulation to analyze the circuit's behavior. Review the output waveforms, voltages, currents, and other relevant parameters to verify the circuit's functionality.
7. **Result Analysis**: Analyze the simulation results to ensure the circuit meets the desired specifications. Adjust the circuit design as needed based on the analysis.
8. **Layout Design (if required)**: For IC design, proceed to the layout editor to create the physical layout of the circuit. Ensure that the layout corresponds accurately to the schematic.
9. **Layout Versus Schematic (LVS) Check**: Perform an LVS check to verify that the layout matches the schematic. This step is crucial to ensure that the physical design accurately implements the intended circuit.
10. **Post-Layout Simulation (if applicable)**: Run post-layout simulations to account for parasitic effects introduced during the layout process. This step ensures the circuit's performance is as expected after layout.

11. **Final Verification and Export**: Once the design is verified, perform a final check, and then export the design files for fabrication or further processing.

These steps were demonstrated during the workshop for designing and verifying the circuit in Cadence.

1. Launch the Cadence Environment
2. 2. Create a New Project/Library
3. Create a Schematic
4. Check and Save the Schematic
5. Create a Testbench (Optional but Recommended)
6. Setup the Simulation
7. Set Simulation Parameters
8. Run the Simulation
9. Analyze the Results
10. Optimization and Further Simulation
11. Post-Simulation Checks

The online workshop titled "Circuit Simulation Using Cadence," led by Dr. Ashima Gupta, provided an in-depth understanding of circuit simulation techniques using the Cadence software suite. The participants gained hands-on experience with various tools within the Cadence platform, which are widely used in the design and analysis of electronic circuits.

Key outcomes of the workshop include

1. Enhanced Knowledge of Circuit Design and Simulation
2. Hands-on Practical Skills
3. Improved Problem-Solving Abilities
4. Industry-Relevant Skills
5. Collaborative Learning Environment

Overall, the workshop equipped attendees with essential skills and knowledge to effectively use Cadence software for circuit simulation, preparing them for future challenges in the field of electronics and circuit design.

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Number of students registered the workshop: - 55 (List attached)

Bholu Gurjar	0901EC221032
Ratnesh Asati	0901EC221087
SUMEET SINGH SENGAR	0901EC221128
Prashant Atal	0901ET231049
Ayush Ratnakar	0901EC221027
Dhruv Shrivastava	0901EC221037
Akansha	0901EC221006
Shweta Singh	0901EC221120
Satyam Gupta	0001EC221109
Nishant Pandey	0901EC221070
Tanish Pali	0901EC221134
Satyam	0901ET231062
Vidhi Dixit	0901EC221150
VIPENDRA BAGHEL	0901EC221153
Himesh Gupta	0901ET221026
Ankit Singh Parihar	0901ET221006
Ashwin Patel	0901ET231015
Vishnu Bansal	0901ET221076
Dileep ahirwar	0901ET221020
Dipanshu Malgaya	0901ET231019
Atharv Shrotriya	0901EC221021
Divyanshi Singh	0901EC221038
Suryansh Dixit	0901EC221130
Priyansi Singh	0901EC211097
Aditi Patel	0901EC211007
Piyush Shrivastava	0901EC211087
Swayam Sahu	0901EC221133
Shivam Parashar	0901EC211108
Hitesh jhala	0901EC211059
Shivraj Singh	0901EC211110
Bhragesh Patel	0901ET221016
Gaurav Rawat	0901ET231020
Aditya Verma	0901EC211013
yash uchhasare	0901ec221156
Sakshi garg	0901EC211102
Prashant Pathak	0901EC221076
Shivansh Singh	0901ET231065
Sanjay Bisariya	0901EC221105
Supriya Gautam	0901EC211121

Gaurav Gautam	0901EC221040
TANISHQ AGRAWAL	0901EC221137
Ayush Agrawal	0901EC221023
Deepansh Shrivastava	0901EC211042
Yashaswini Tyagi	0901EC211138
Rudra Sharma	0901EC221095
Vivek Prajapati	0901EC221154
Viraj Gupta	0901ET231076
Tejendra Bansal	0901ec221141
Tilak Rajak	0901EC211127
Satyam dubey	0901ET231063
Amit Kumar Vishviya	0901EC211020
Pooja Sahu	0901EC211088
Himanshi Kankane	0901EC211058
Nishkarsh Sharma	0901ET221041
Lavin Panchgavkar	0901ET231033
NITIN SHARMA	0901EC211084

Enclosure-

1. Photos

Prateek Bhadauria
Coordinator,
Assistant Professor

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Photo during workshop