MADHAV INSTITUTE OF TECHNOLOGY & SCIENCE, GWALIOR (M.P.)

A Govt. Added UGC Autonomous and NAAC Accredited Institute, Affiliated to R.G.P.V, Bhopal

DEPARTMENT OF ELECTRONICS ENGINEERING

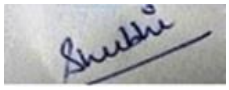
Multiple Mode Teaching Learning Pattern

Name of Course with Code: VLSI Design (140603)	**Class:** B. Tech. III Year	**Session:** Jan-June 2023

S. No.	Unit	Content to be Covered	Teaching Session	Mode
1.	Unit 1	The Metal Oxide Semiconductor (MOS) Structure	1	Offline&Opendiscussions
2.		The MOS System under External Bias, Structure and Operation of MOS Transistor (MOSFET)	2-3	Offline & problem solving based learning
3.		MOSFET Current-Voltage Characteristics	4-5	Offline & problem solving based learning
4.		MOSFET Scaling and Small-Geometry Effects	6-7	Offline & problem solving based learning
5.		MOSFET Capacitances.	8-9	Offline & problem solving based learning
6.	Unit 2	Introduction, Voltage Transfer Characteristic (VTC)	10	Offline & problem solving based learning
7.		Noise Immunity and Noise margins Resistive-Load Inverter, Inverters with n-Type MOSFET Load and CMOS Inverter,	11-12	Offline & problem solving based learning
8.		DC Characteristics of CMOS Inverter, Calculation of VIL, VIH, VOL, VOH and Vth, Design of CMOS Inverters	13-14	Offline & problem solving based learning
9.		Supply Voltage Scaling in CMOS Inverters, Power and Area considerations.	15	Offline & problem solving based learning
10.	Unit 3	Switching Characteristics of CMOS Inverter- Delay-Time Definitions	16	Online&demonstrationbase dlearning
11.		CMOS Propagation Delay	17	Online&demonstrationbase dlearning
12.		Calculation of Delay times, Power Dissipation-Switching	18-19	Offline & problem solving based learning
13.		Short-Circuit and Leakage Components of Energy and Power, Power-Delay Product	20-24	Offline & problem solving based learning
14.		Combinational MOS logic circuits	25	Online&demonstrationbase dlearning
15.		CMOS Logic circuits (NAND, NOR and Complex Logic Gates, Multiplexers etc.)	26	Offline & problem solving based learning

16.	**Unit 4**	CMOS Transmission Gates (Pass Gates), CMOS n-Well Process,	27-29	Offline & problem solving based learning
17.		Layout design rules, layout design of CMOS Inverter, designing of stick diagram.	30-31	Offline&demonstrationbasedlearning
18.	**Unit 5**	Semiconductor memories: non-volatile and volatile memory devices, flash memories	32	Offline&Open discussions
19.		SRAM cell design,	33	Offline & problem solving based learning
20.		1T DRAM cell design, dynamic CMOS logic circuits ,domino logic CMOS circuits	34-35	Offline & problem solving based learning

Online	Offline						
	BlackBoardTeaching	GroupbasedLearning	Learningthroughprojects	Learningthroughdemonstration	Learningthroughexperimentation	ActivitybasedLearning	Onsite/fieldbasedlearning
13.22%	85.71%	37.21%	13.95	27.90%	48.84.%	13.95%	-%



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